What is claimed is:

1. A image sensor with a vertically integrated thin-film photodiode, comprising:

a substrate;

an interconnection structure adjacent to the substrate, wherein the interconnection structure includes a top metal layer comprising a plurality of first metal pads for thin-film photodiodes and a second metal pad for a ground pad;

a dielectric layer with a plurality of first openings and a second opening disposed on the interconnection structure;

a plurality of bottom doped layers with a first conductive type respectively disposed in the first openings, wherein each bottom doped layer contacts the corresponding first metal pad without extending outside the surface of the corresponding first metal pad;

an I-type layer disposed over at least one bottom doped layer and the dielectric layer;

an upper doped layer with a second conductive type disposed over the I-type layer; and

a transparent electrode disposed over the upper doped layer and contacting the second metal pad through the second opening in the dielectric layer.

2. The image sensor with a vertically integrated thin-film photodiode of claim 1, wherein the thin-film photodiodes are PIN photodiodes.

3. The image sensor with a vertically integrated thin-film photodiode of claim 1, further comprising a passivation layer covering the transparent electrode and the dielectric layer.

4. The image sensor with a vertically integrated thin-film photodiode of claim 3, further comprising a bonding opening passing through the passivation layer and the dielectric layer to the second metal pad.

5. The image sensor with a vertically integrated thin-film photodiode of claim 1, wherein the size of each first opening is about 0.5μm × 0.5μm ~ 20μm × 20μm.

6. The image sensor with a vertically integrated thin-film photodiode of claim 1, wherein each bottom doped layer is conformally disposed in the corresponding first opening.

7. A image sensor with a vertically integrated thin-film photodiode, comprising:

a substrate having a ground pad region, a pixel array region and a ASIC circuit region;

an interconnection structure adjacent to the substrate, wherein the interconnection structure includes a top metal layer comprising a plurality of pixel electrodes in the pixel array region, a ground pad in the ground pad region and a circuit pad in the ASIC circuit region;

a dielectric layer with a plurality of first openings and a second opening disposed on the

interconnection structure, wherein a bottom of each first opening is a surface of the corresponding pixel electrode;

a plurality of bottom doped layers with a first conductive type respectively disposed in the first openings, wherein each bottom doped layer contacts the corresponding pixel electrode;

an I-type layer disposed over at least one bottom doped layer and the dielectric layer;

an upper doped layer with a second conductive type disposed over the I-type layer; and

a light transmitting electrode disposed over the upper doped layer and contacting the second metal pad through the second opening in the dielectric layer.

8. The image sensor with a vertically integrated thin-film photodiode of claim 7, wherein the thin-film photodiodes are PIN photodiodes.

9. The image sensor with a vertically integrated thin-film photodiode of claim 7, further comprising a passivation layer covering the light transmitting electrode and the dielectric layer.

10. The image sensor with a vertically integrated thin-film photodiode of claim 9, further comprising a first bonding opening passing through the passivation layer and the dielectric layer to the ground pad, and a second bonding opening passing through the passivation layer and the dielectric layer to the circuit pad.

11. The image sensor with a vertically integrated thin-film photodiode of claim 7, wherein the size of each first opening is about 0.5μm × 0.5μm ~ 20μm × 20μm.

12. The image sensor with a vertically integrated thin-film photodiode of claim 7, wherein each bottom doped layer is conformally disposed in the corresponding first opening.

13. A method for forming an image sensor with a vertically integrated thin-film photodiode, comprising:

providing a substrate;

forming an interconnection structure adjacent to the substrate, wherein the interconnection structure includes a top metal layer comprising a plurality of first metal pads for thin-film photodiodes and a second metal pad for a ground pad;

forming a dielectric layer on the interconnection structure;

forming a plurality of first openings and a second opening in the dielectric layer;

forming a plurality of bottom doped layers with a first conductive type in the first openings and the second opening, wherein each bottom doped layer contacts the corresponding first metal pad without extending outside the surface of the corresponding first metal pad;

forming a stacked layer of an I-type layer and an upper doped layer with a second conductive type over at least one bottom doped layer and the dielectric layer;

removing the bottom doped layer in the second opening;

forming a transparent electrode over the upper doped layer and contacting the second metal pad through the second opening in the dielectric layer.

14. The method for forming the image sensor with a vertically integrated thin-film photodiode of claim 13, wherein the method of forming the bottom doped layers comprises:

forming a layer doped with the first conductive type conformally on the dielectric layer and in the first and second openings;

coating an organic spin-on material on the layer doped with the first conductive type with a substantially flat plane;

removing the organic spin-on material and the layer doped with the first conductive type until the upper surface of the dielectric layer is exposed, wherein the dielectric layer, and upper surfaces of the organic spin-on material and the layer doped with the first conductive type in the first and second openings together form a substantially planar surface; and

removing the remaining organic spin-on material.

15. The method for forming the image sensor with a vertically integrated thin-film photodiode of claim 14, wherein the method of removing the organic spin-on material and the layer doped with the first conductive type until the upper surface of the dielectric layer is exposed is etching back.

16. The method for forming the image sensor with a vertically integrated thin-film photodiode of claim 13, wherein the method of forming the stacked layer of the I-type layer and the upper doped layer over at least one bottom doped layer and the dielectric layer comprises:

forming a layer of I-type material on the bottom doped layers and the dielectric layer;

forming a layer of second conductive type material on the layer of I-type material; and

patterning the layer of second conductive type material and the layer of I-type material to form the stacked layer of the I-type layer and the upper doped layer with the second conductive type.

17. A method for forming an image sensor with a vertically integrated thin-film photodiode, comprising:

providing a substrate having a ground pad region, a pixel array region and a ASIC circuit region;

forming an interconnection structure adjacent to the substrate, wherein the interconnection structure includes a top metal layer comprising a plurality of pixel electrodes in the pixel array region, a ground pad in the ground pad region and a circuit pad in the ASIC circuit region;

forming a dielectric layer on the interconnection structure;

forming a plurality of first openings and a second opening in the dielectric layer, wherein a bottom of each first opening is a surface of the corresponding pixel electrode;

forming a plurality of bottom doped layers with a first conductive type in the first openings and the second opening, wherein each bottom doped layer contacts the corresponding pixel electrode;

forming a stacked layer of an I-type layer and an upper doped layer with a second conductive type over at least one bottom doped layer and the dielectric layer;

removing the bottom doped layer in the second opening;

forming a light transmitting electrode over the upper doped layer and contacting the second metal pad through the second opening in the dielectric layer.

18. The method for forming the image sensor with a vertically integrated thin-film photodiode of claim 17, wherein the method of forming the bottom doped layers comprises:

forming a layer doped with the first conductive type conformally on the dielectric layer and in the first and second openings;

coating an organic spin-on material on the layer doped with the first conductive type with a substantially flat plane;

removing the organic spin-on material and the layer doped with the first conductive type until the upper surface of the dielectric layer is exposed, wherein the dielectric layer, and upper surfaces of the organic spin-on material and the layer doped with the first conductive type in the first

and second openings together form a substantially planar surface; and

removing the remaining organic spin-on material.

19. The method for forming the image sensor with a vertically integrated thin-film photodiode of claim 18, wherein the method of removing the organic spin-on material and the layer doped with the first conductive type until the upper surface of the dielectric layer is exposed is etching back.

20. The method for forming the image sensor with a vertically integrated thin-film photodiode of claim 17, wherein the method of forming the stacked layer of the I-type layer and the upper doped layer over at least one bottom doped layer and the dielectric layer comprises:

forming a layer of I-type material on the bottom doped layers and the dielectric layer;

forming a layer of second conductive type material on the layer of I-type material; and

patterning the layer of second conductive type material and the layer of I-type material to form the stacked layer of the I-type layer and the upper doped layer with the second conductive type.